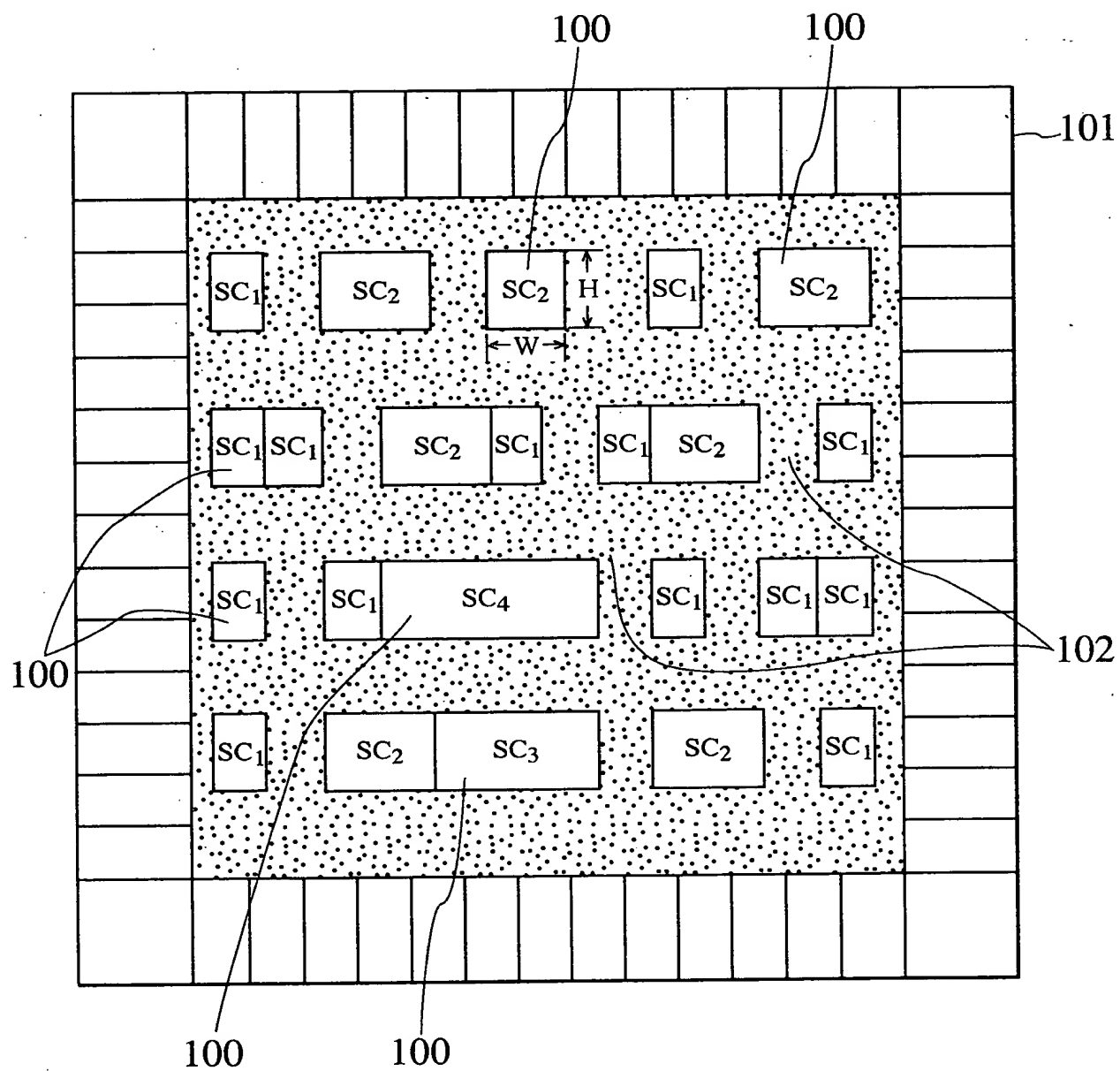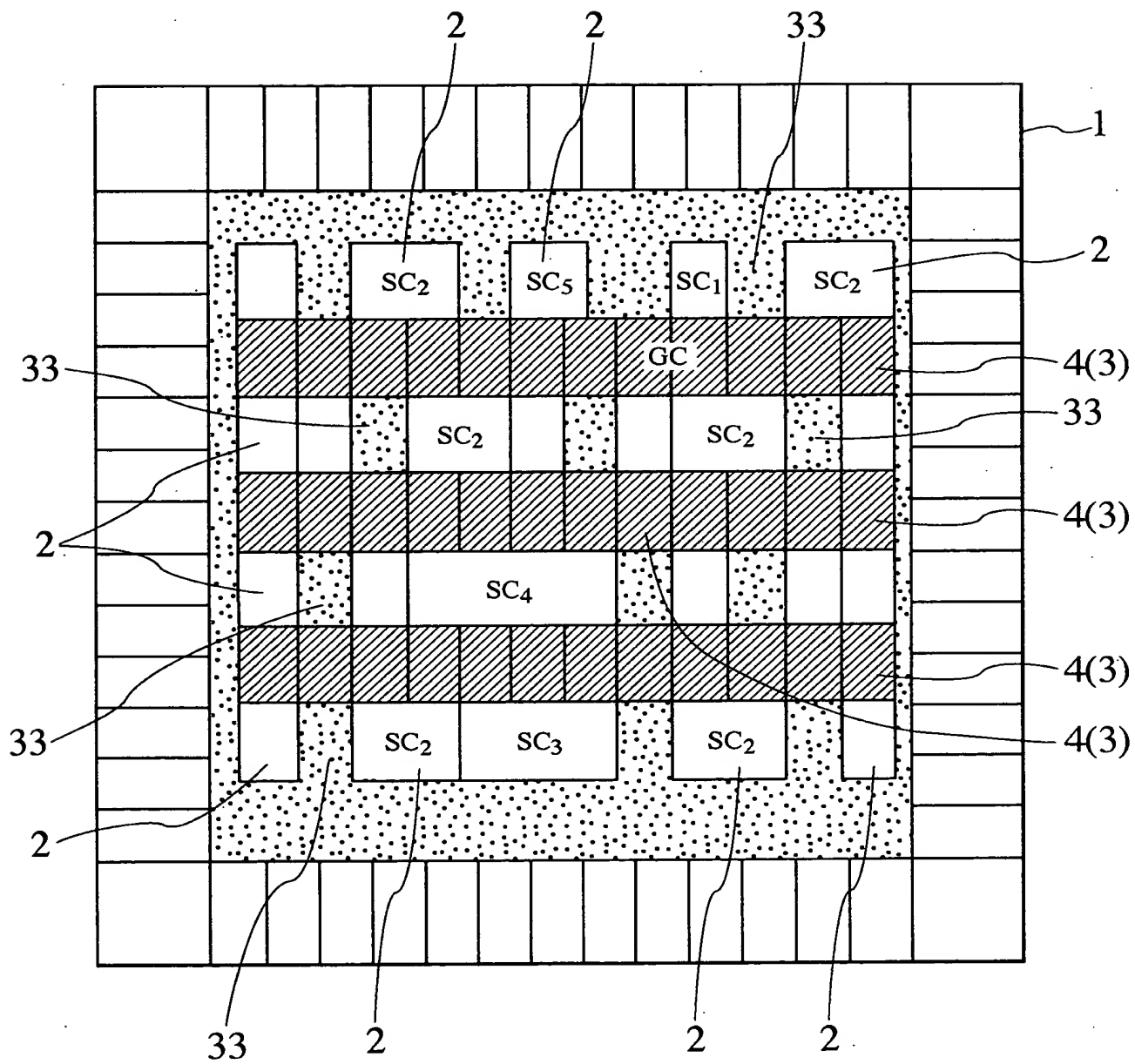6054872

FIG. 1

PRIOR ART

FIG. 2

PRIOR ART
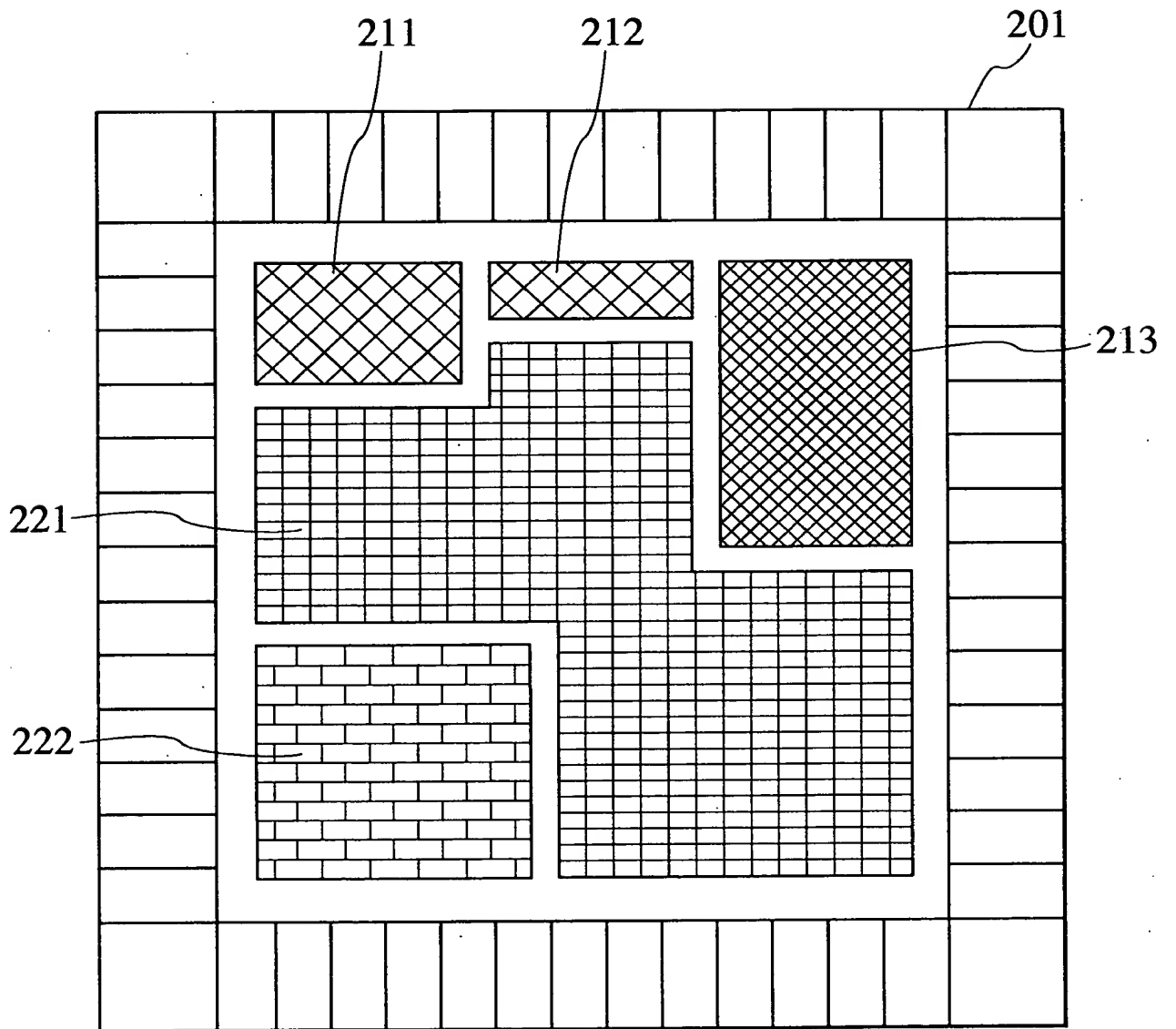
FIG. 3A

FIG. 3B

FIG. 3C

FIG. 3D

FIG. 4A

54
52
53
56
55
57
58
51

CLOCK
DRIVER

1

FIG. 4B

2
4
4
2
2
1

CLOCK
DRIVER

FIG. 5A

FIG. 5B

This figure is a semiconductor device layout diagram with numerous labeled regions including: 98, VDD 9, n, 71D, 381, 383, 351, 384, 385, p, 72D, Vss 10, 97, 71S 61, Q1, 382, 352, 72S, Q2, 62, 386, 73, p+, n+, X, 74, n+, p+, n+, n+, 6, 75S 75S, 354 64 392, Q3, 393, 394, 77, 353, 398, 76S, A, 75D, 391, 395, 76D, 76S, 399 355, 75S, Q4, Q6, 396, 78, p 397, 76S, B, 63, n, 5, 96, 95, H
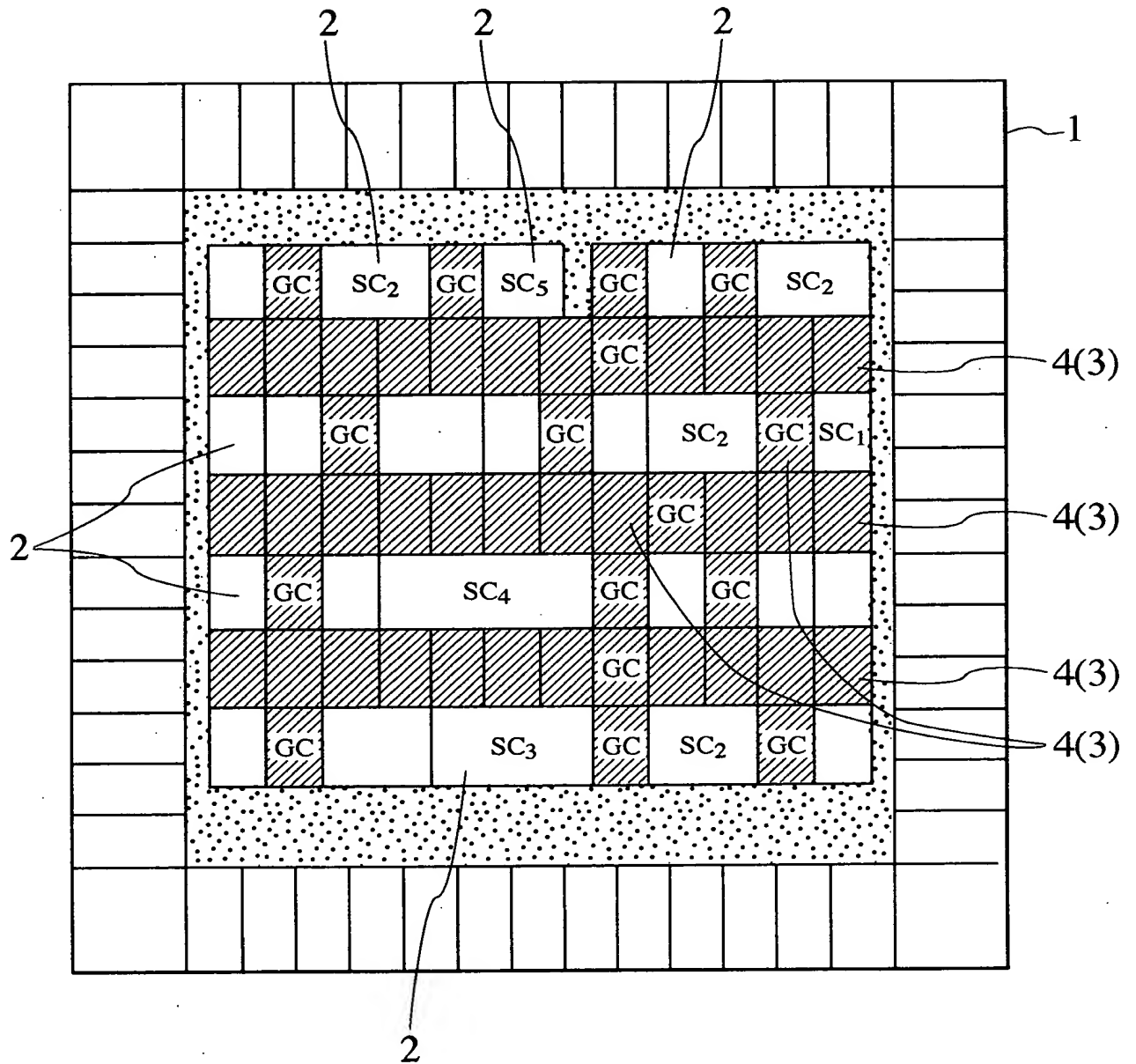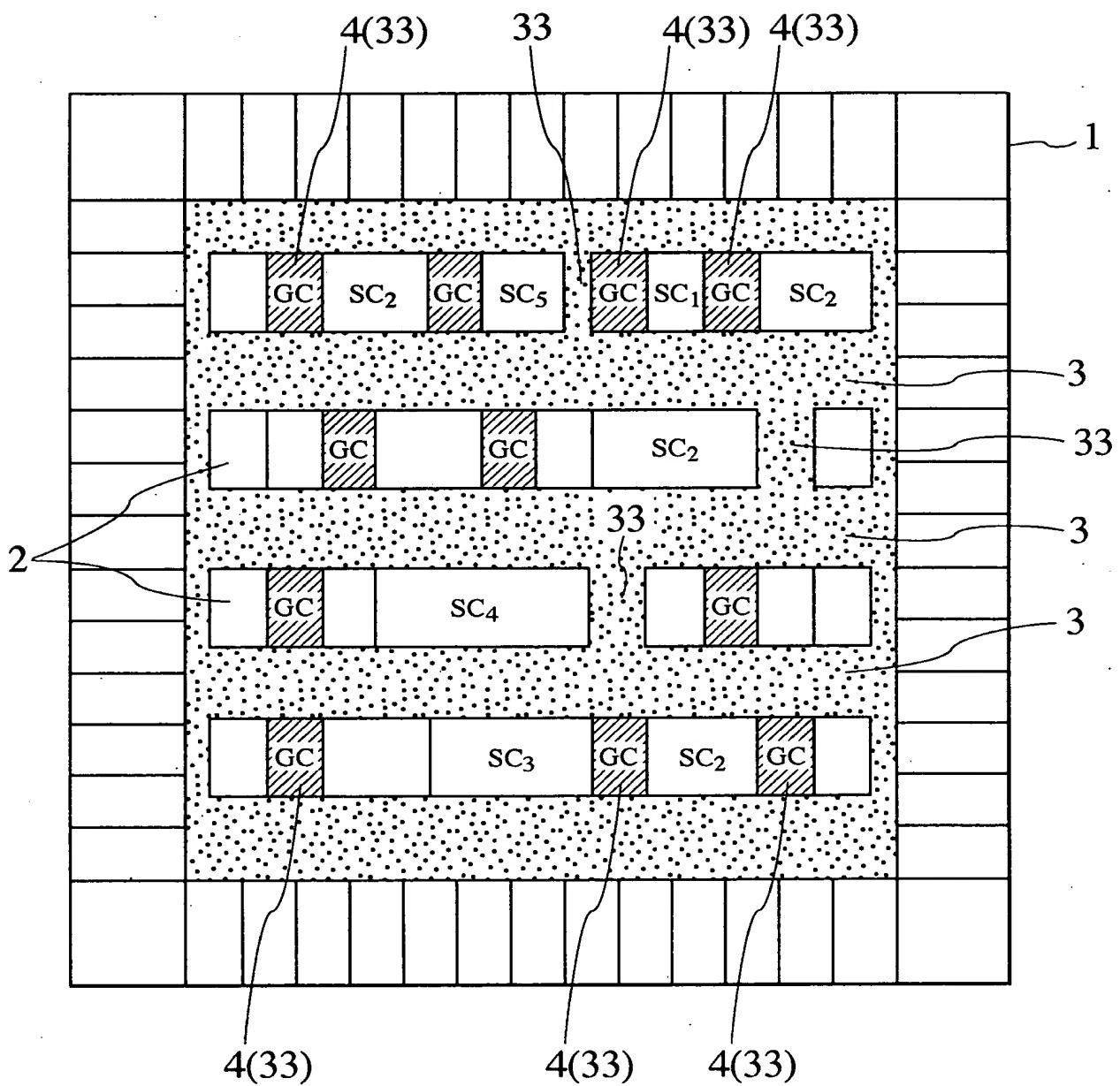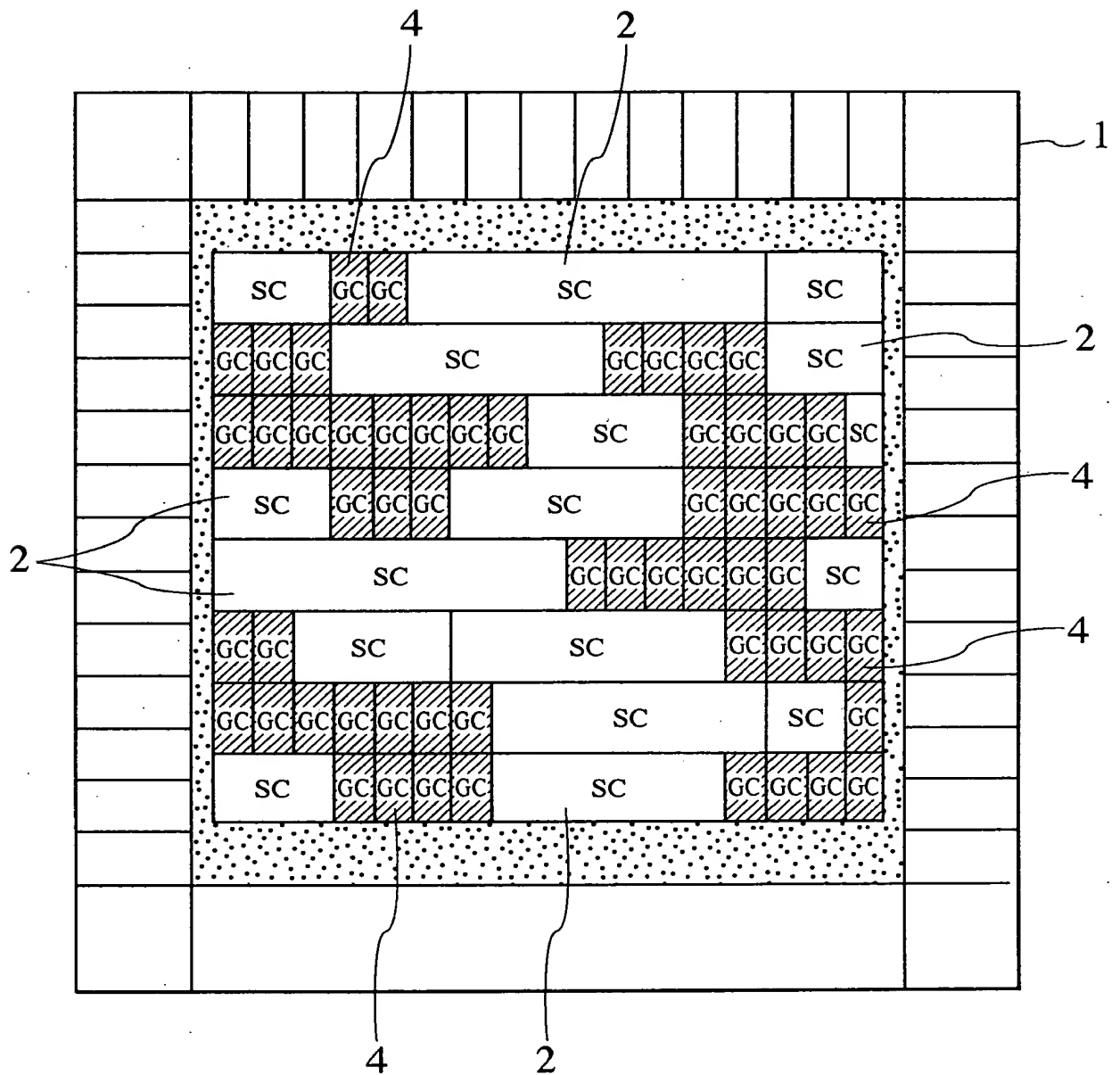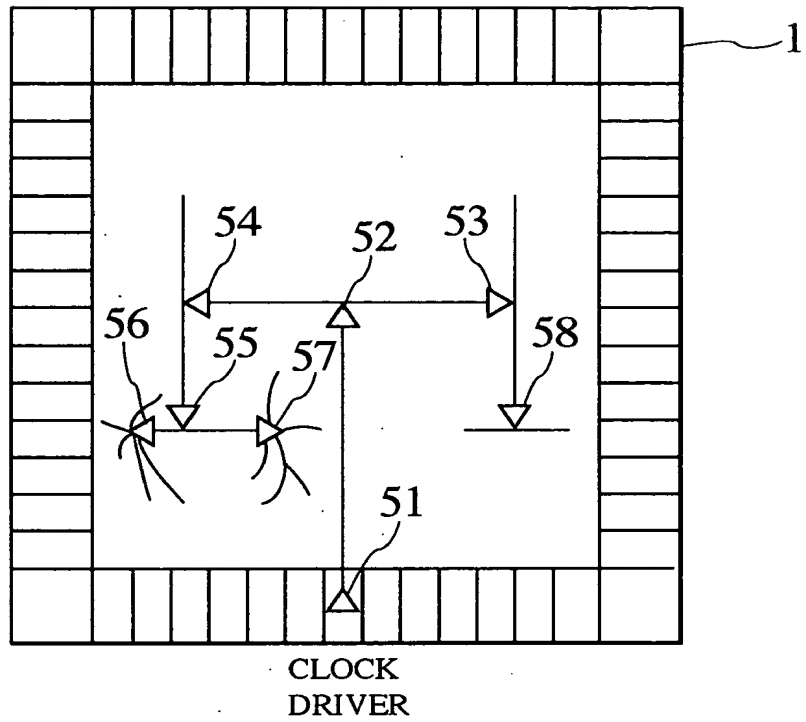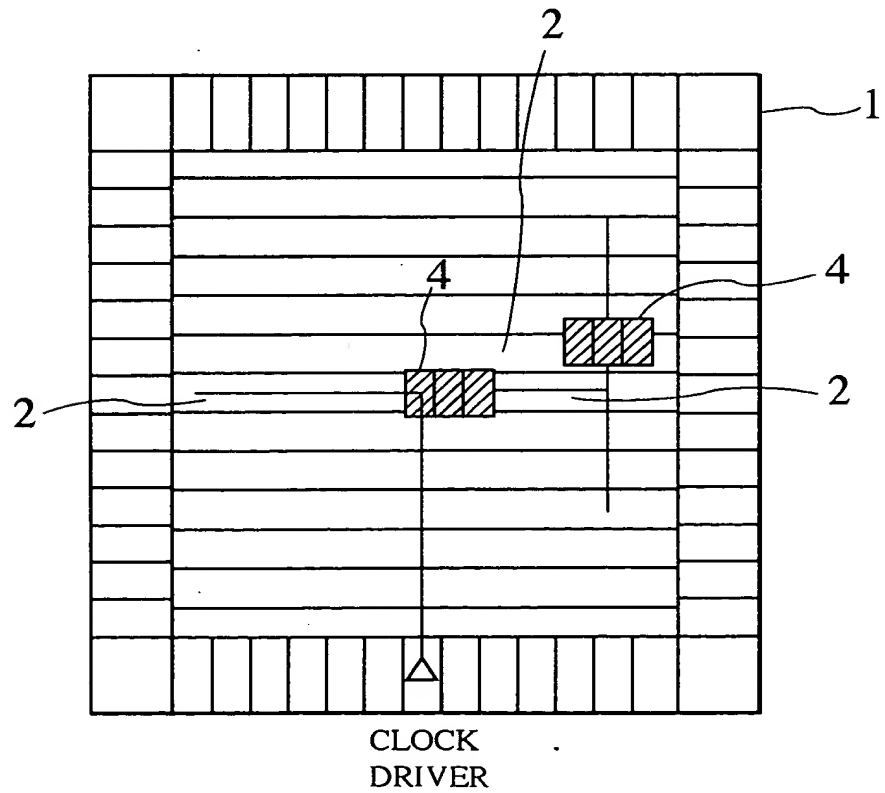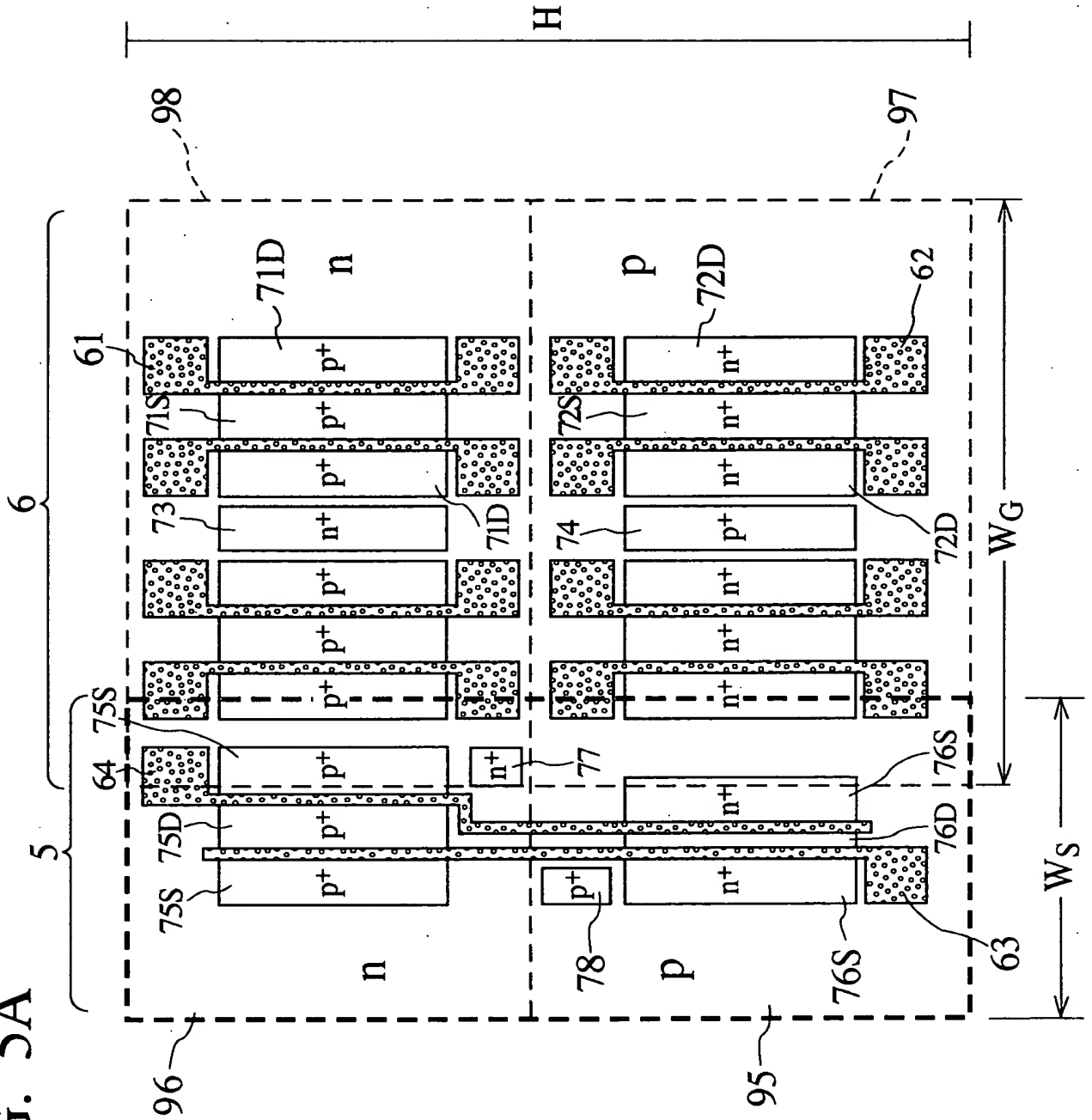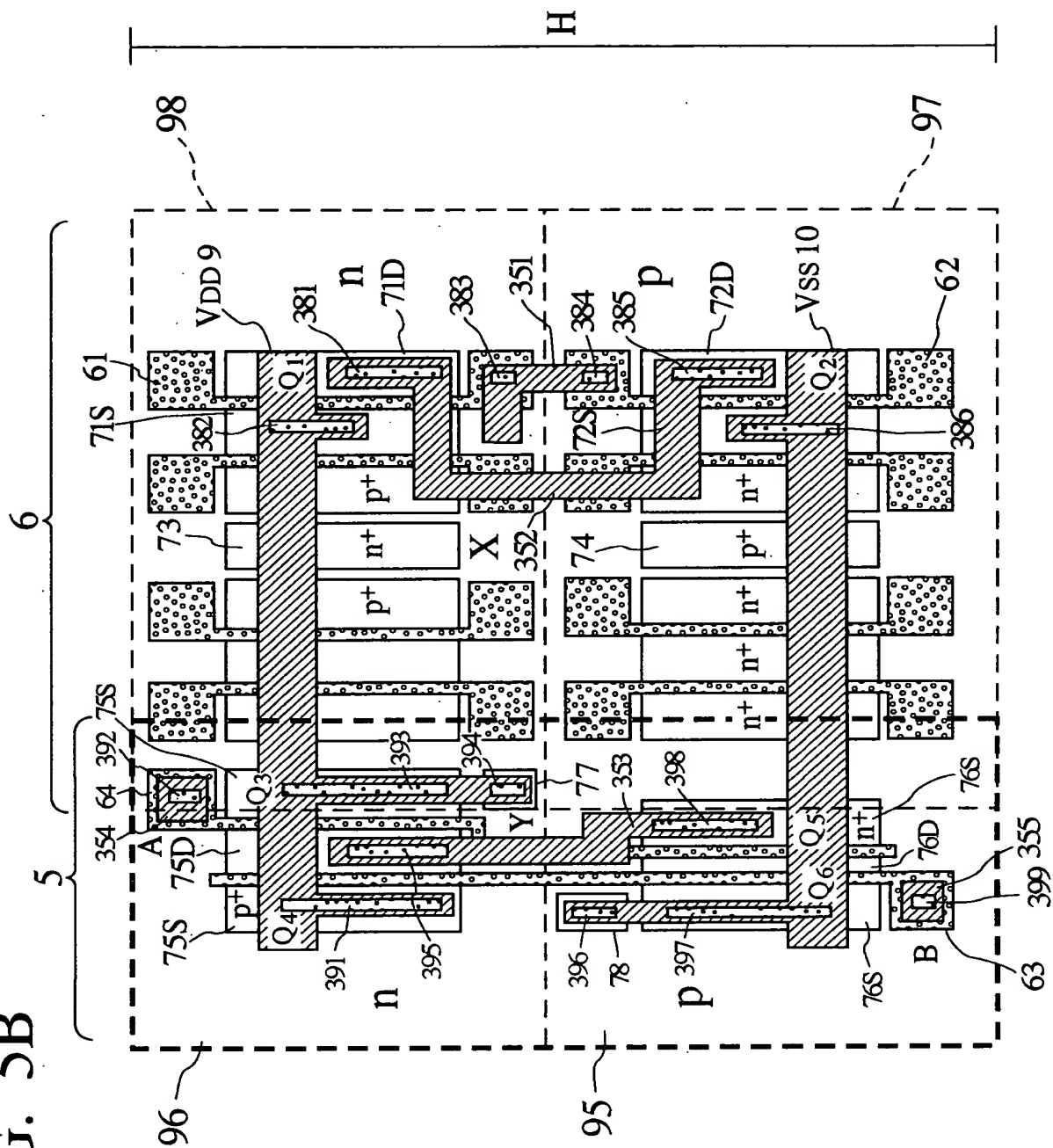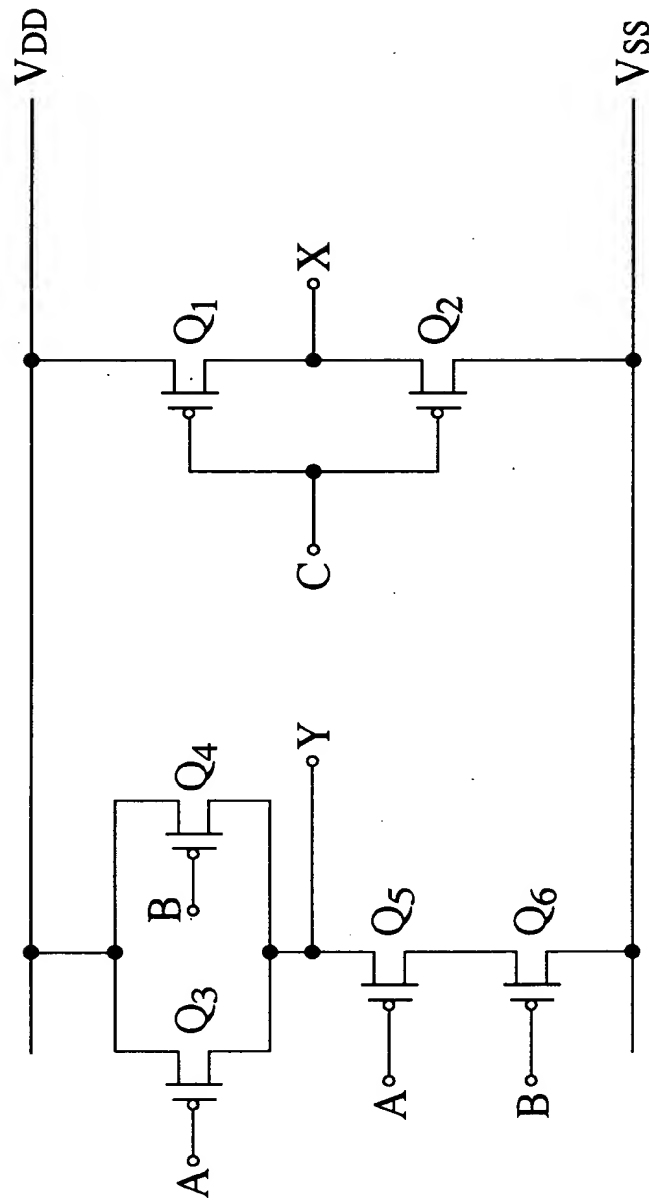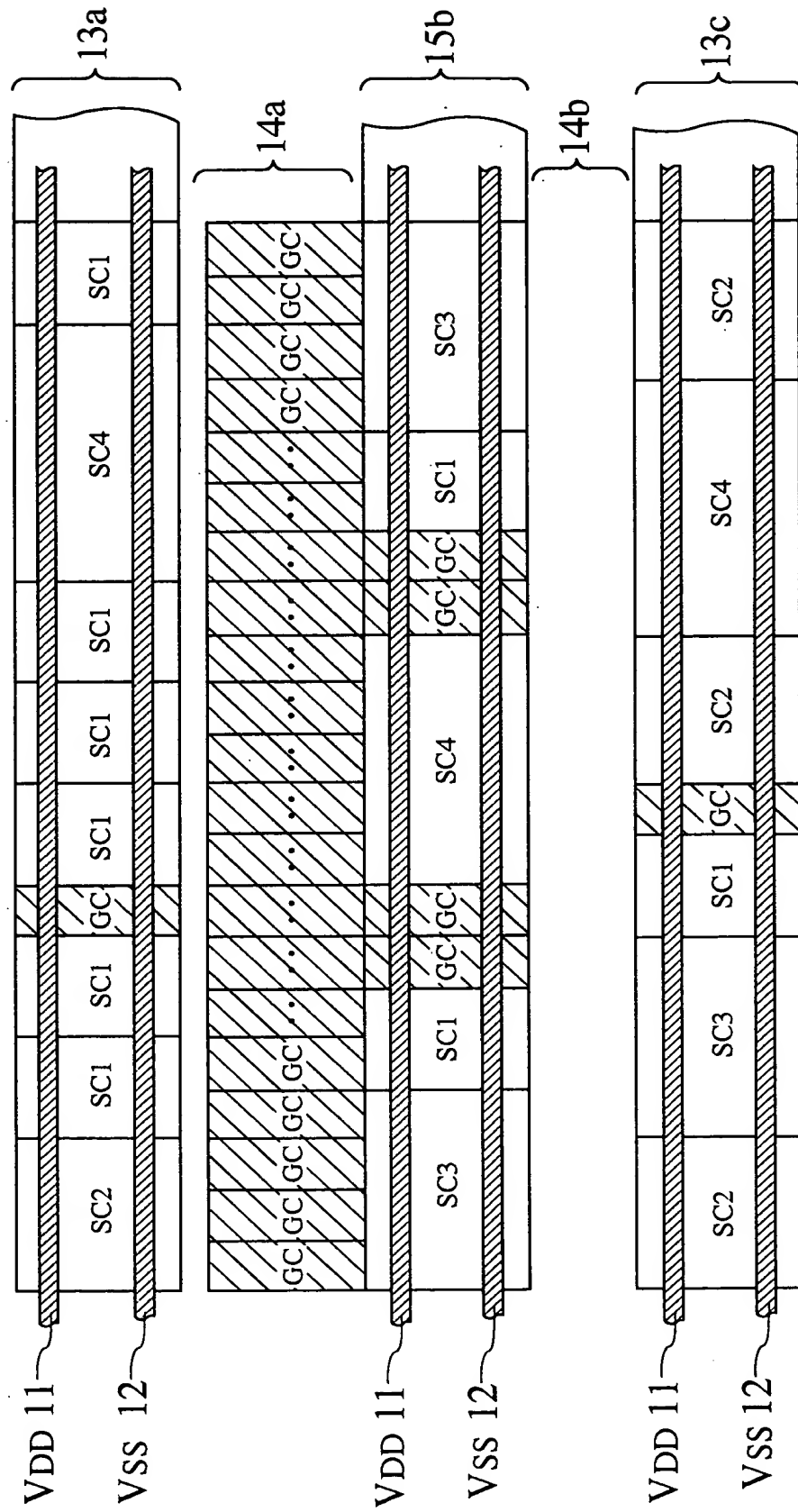
FIG. 5C

FIG. 6

FIG. 7
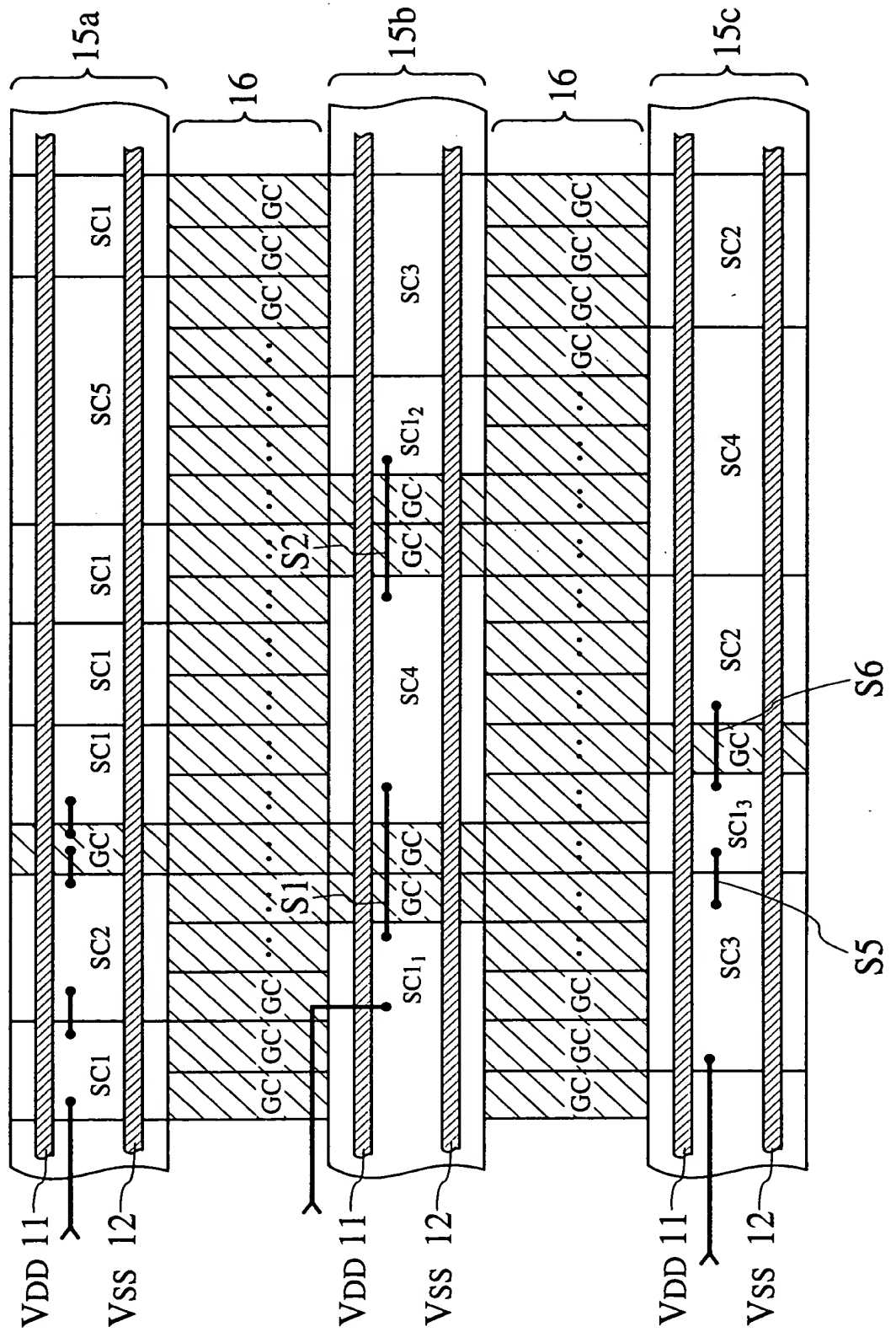
FIG. 8
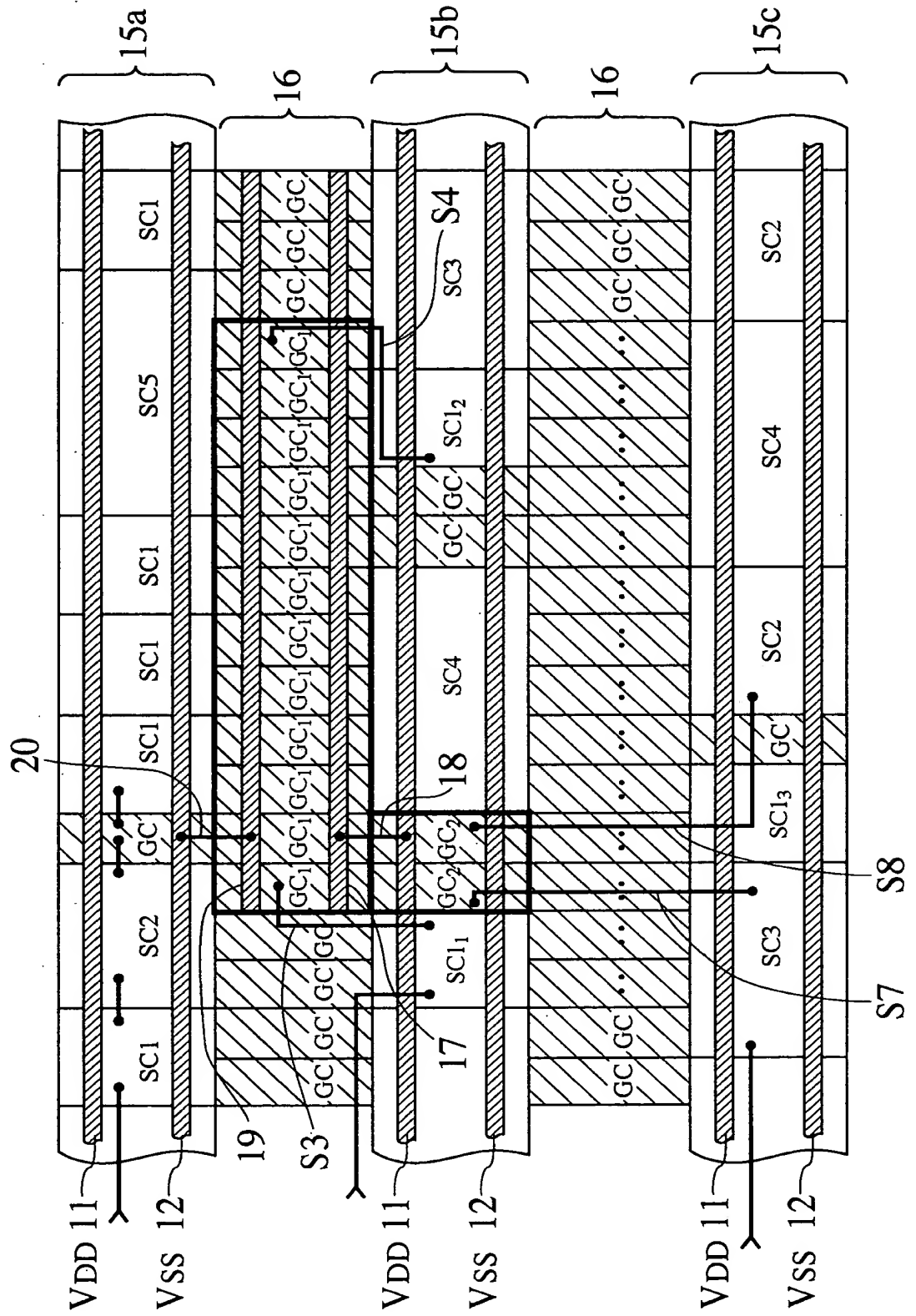
FIG. 9

FIG. 10A

FIG. 10B

FIG. 11